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09/734,856	12/12/2000	Masatsugu Takeuchi	FUJI 18.099	4740

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EXAMINER	
PERILLA, JASON M	
ART UNIT	**PAPER NUMBER**
2638	

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/734,856	TAKEUCHI ET AL.	
	Examiner	Art Unit	
	Jason M. Perilla	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,7,8 and 10* is/are rejected.

7)☐ Claim(s) *4-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-8 and 10 are pending in the instant application.

Response to Amendment/Arguments

2. Applicant's arguments, see page 8, filed July 20, 2005, with respect to the rejection(s) of claim(s) 1, 3, and 7 under 35 U.S.C. § 102(b) as being anticipated by Hennedy et al (US 5999562) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Hennedy et al.

It is noted by the Examiner that the prior art reference Hennedy et al discloses a code register as claimed but does not *explicitly* disclose that the code register includes first and second code registers as required in an application of 35 U.S.C. § 102(b). However, the Examiner finds, as set forth below, that first and second code registers is implied or at least obvious in view of the disclosure of Hennedy et al. Therefore, new prior art rejections are set forth below.

Further, new prior art rejections are set forth in view of the prior art reference Tran et al (US 5715276).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3, 7, and 10 are rejected under 35 U.S.C. §102(b) as being anticipated by Tran et al (US 5715276; hereafter "Tran" – previously cited).

Regarding claim 1, Tran discloses by figure 16 an apparatus, comprising: a plurality of received-signal registers (255; I IN, 244 Q IN) which receive and store therein a plurality of respective received-signal sequences (col. 24, lines 2-5); a selector (233) which selects one of the received signal sequences stored in said received-signal registers (col. 24, lines 5-6); at least one code register (131, 132) which stores therein a de-spreading-code sequence (col. 24, lines 18-20, lines 30-33), a multiplication circuit (235) which multiplies the selected one of the received-signal sequences by the de-spreading-code sequence; and a summation circuit (137, 138, and 139) which obtains a sum of results of the multiplication to obtain a correlation between the selected one of the received-signal sequences and the de-spreading-code sequence (col. 24, lines 13-15); wherein said at least one code register includes a first code register (132) storing a first de-spreading code and a second code register (131) storing a second de-spreading code.

Regarding claim 3, Tran discloses the limitations of claim 1 as applied above. Further, Tran discloses a delay profile-holding circuit (fig. 1, ref. 41) which generates a delay profile (fig. 3) based on correlations obtained by the summation circuit (col. 8, lines 39-65); and a path timing detection circuit (fig. 1, ref. 46) which detect a path timing by detecting a peak of the delay profile (col. 8, lines 13-20).

Regarding claim 7, Tran discloses an apparatus for obtaining a correlation by figure 16 wherein a correlation calculating unit calculates the correlation while shifting,

relative to a de-spreading code, a phase of a received signal spread by a spreading code, comprising; a first shift register (255) configured to store a first received signal; a second shift register (256) configured to store a second received signal; a selector unit (233) configured to selectively output one of the first received signal and the second received signal; and a control unit (fig. 1, ref. 46) configured to cause said selector unit to output the first received signal and to cause the correlation calculating unit to calculate a correlation with respect to the first received signal, followed by causing said selector unit to output the second received signal and by causing the correlation calculating unit to calculate a correlation with respect to the second received signal (col. 14, lines 55-63); wherein the first received signal is a signal spread by a first spreading code and the second received signal is a signal spread by a second spreading code, said apparatus further comprising: a de-spreading code selecting unit (133) configured to select a first de-spreading code (132) corresponding to the first spreading code for correlation calculation of the first received signal, and to select a second de-spreading code (132) corresponding to the second spreading code for correlation calculation of the second received signal, such that each of a pattern of the first spreading code and a pattern of the second spreading code are different; wherein said first de-spreading code originates from a first code register (131) and said second de-spreading code originates from a second code register (132).

Regarding claim 10, Tran discloses, according to claim 7 above, the limitations of the claim including a first shift register, a second shift register, a selector unit, and a control unit. Further, Tran discloses according to figure 1 that a received signal

(SIGNAL INPUT) is divided into first (in-phase) and second (quadrature) signals (outputs of mixers 31 and 32) and each divided signal is sampled by a sampler (33 and 34). Tran further discloses, according to the illustrations of figure 1 and 16, that the first and second divided signals become the first and second received signals (fig. 16; I IN and Q IN, respectively) after being sampled. Where the first and second (fig. 1, outputs of mixers 31 and 32) signals are components of the "SIGNAL INPUT" of figure 1, they are considered to be "oversampled" by the two sampling analog to digital converters (fig. 1, refs. 33 and 34) because they are sampled *two-fold* with respect to the single SIGNAL INPUT and are picked every few samples of the composite SIGNAL INPUT to create the two sequences of the first and second received signals (outputs of the analog to digital converters 33 and 34, respectively). Additionally, the correlation calculations of the first received signal and the second received signal are performed by use of a common de-spreading code (fig. 16, 131, 132).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 8 is rejected under 35 U.S.C. §103(a) as being unpatentable over Tran.

Regarding claim 8, Tran discloses the limitations of claim 7 as applied above. Tran does not explicitly disclose that the second shift register shifts the second received signal to set the second received signal to a predetermined phase while correlation

calculation is being performed for the first received signal. However, Tran teaches that in the multiplex correlator as illustrated in figures 1, and 16, the in-phase and quadrature received signals must be in alignment with the local in-phase and quadrature signals for correlation to be performed (col. 17, lines 19-24). That is, before correlation may be performed, the signals in the shift registers must be at a predetermined phase alignment. Tran teaches that the use of the multiplexed arrangement saves physical volume and power (col. 17, lines 35-40), but requires that the shift registers must be fully loaded and in the correct phase alignment for correlation (col. 17, lines 24-30). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to align the second received signal register to a predetermined phase while correlation is being performed on the first received signal because it would allow for correlation of the second received signal to be preformed correctly and immediately after the first received signal is correlated as taught and implied by Tran.

7. Claims 1, 3, 7, 8 and 10 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hennedy et al (US 5999562; hereafter "Hennedy" – previously cited).

Regarding claim 1, Hennedy discloses by figure 8 an apparatus, comprising: a plurality of received-signal registers (I SIGNAL, Q SIGNAL REG.) which receive and store therein a plurality of respective received-signal sequences (col. 25, lines 35-41); a selector (MULTIPLEXER) which selects one of the received signal sequences stored in said received-signal registers (col. 25, lines 60-65); at least one code register (DATA REFERENCE SIGNAL REGISTER) which stores therein a de-spreading-code

sequence (col. 26, line 15, col. 28, lines 4-11), a multiplication circuit (XOR gates) which multiplies the selected one of the received-signal sequences by the de-spreading-code sequence (col. 26, lines 20-25, 60-65); and a summation circuit (AND gates) which obtains a sum of results of the multiplication to obtain a correlation between the selected one of the received-signal sequences and the de-spreading-code sequence. Hennedy does not explicitly disclose that said at least one code register includes a first code register storing a first de-spreading code and a second code register storing a second de-spreading code. However, Hennedy does disclose that the code register stores distinct "I_SIG code" and "Q_SIG code" (col. 27, lines 60-65) codes. Further, Hennedy discloses that the pattern of the first de-spreading code and the pattern of the second de-spreading code are different, and said apparatus further comprising a selector (MULTIPLEXER) which selects one of said first code and said second code to select and supply the de-spreading-code sequence to the multiplication circuit. While the at least one code register as illustrated in figure 8 of Hennedy is shown as a single code register coupled to a multiplexer, it is obvious to one having skill in the art that the "DATA REFERENCE SIGNAL REGISTER" (fig. 8) is functionally equivalent to two separate (a first and a second) code signal registers. For instance, a multiplexer is coupled to the data reference signal register to choose an independent reference signal depending upon a correlation to occur with the I or Q received signal. Therefore, the "DATA REFERENCE SIGNAL REGISTER" is *functionally* separated into two separate code signal registers. Further, Hennedy discloses that the matched filter apparatus illustrated in figure 8 performs correlations of two independent signals by multiplexing its

operations (col. 25, lines 60-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the "DATA REFERENCE SIGNAL REGISTER" of Hennedy could be considered to be, or implemented as, two separate and distinct code registers (that is, a first and a second) because its output *is functionally divided into two separate and distinct outputs* by the multiplexer according to the operation of the apparatus.

Regarding claim 3, Hennedy discloses the limitations of claim 1 as applied above. Further, Hennedy discloses a delay profile-holding circuit (fig. 1, ref. 41) which generates a delay profile (fig. 3) based on correlations obtained by the summation circuit (col. 12, lines 55-65); and a path timing detection circuit (fig. 1, ref. 46) which detect a path timing by detecting a peak of the delay profile (col. 12, lines 5-12).

Regarding claim 7, Hennedy discloses an apparatus for obtaining a correlation by figure 8 wherein a correlation calculating unit calculates the correlation while shifting, relative to a de-spreading code, a phase of a received signal spread by a spreading code, comprising; a first shift register (I SIGNAL REGISTER) configured to store a first received signal (col. 25, lines 35-40); a second shift register (Q SIGNAL REGISTER) configured to store a second received signal (col. 25, lines 35-40); a selector unit (MULTIPLEXER) configured to selectively output one of the first received signal and the second received signal (col. 25, lines 60-65); and a control unit (fig. 1, ref. 46) configured to cause said selector unit to output the first received signal and to cause the correlation calculating unit to calculate a correlation with respect to the first received signal, followed by causing said selector unit to output the second received signal and

by causing the correlation calculating unit to calculate a correlation with respect to the second received signal (col. 29, lines 9-15); wherein the first received signal is a signal spread by a first spreading code and the second received signal is a signal spread by a second spreading code (i.e. "independent; col. 25, lines 60-65), said apparatus further comprising: a de-spreading code selecting unit (MULTIPLEXER) configured to select a first de-spreading code "I_SIG code" (col. 27, lines 60-65) corresponding to the first spreading code for correlation calculation of the first received signal, and to select a second de-spreading code "Q_SIG code" (col. 27, lines 60-65) corresponding to the second spreading code for correlation calculation of the second received signal, such that each of a pattern of the first spreading code and a pattern of the second spreading code are different. Hennedy does not explicitly disclose that said first de-spreading code originates from a first code register and said second de-spreading code originates from a second code register but instead discloses that the "I_SIG code" and "Q_SIG code" each originates from a from a single "DATA REFERENCE SIGNAL REGISTER" (fig. 8). However, as applied to claim 1 above, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the "DATA REFERENCE SIGNAL REGISTER" of Hennedy could be considered to be, or implemented as, two separate and distinct code registers (that is, a first and a second) because its output *is functionally divided into two separate and distinct outputs* by the multiplexer according to the operation of the apparatus.

Regarding claim 8, Hennedy discloses the limitations of claim 7 as applied above. Hennedy does not explicitly disclose that the second shift register shifts the

second received signal to set the second received signal to a predetermined phase while correlation calculation is being performed for the first received signal. However, Hennedy teaches that in the multiplex correlator as illustrated in figures 1, 2, and 8, the in-phase and quadrature received signals must be in alignment with the local in-phase and quadrature signals for correlation to be performed (col. 21, lines 10-16). That is, before correlation may be performed, the signals in the shift registers must be at a predetermined phase alignment. Hennedy teaches that the use of the multiplexed arrangement saves physical volume and power (col. 21, lines 29-31), but requires that the shift registers must be fully loaded and in the correct phase alignment for correlation (col. 21, lines 16-25). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to align the second received signal register to a predetermined phase while correlation is being performed on the first received signal because it would allow for correlation of the second received signal to be preformed correctly and immediately after the first received signal is correlated as taught and implied by Hennedy.

Regarding claim 10, Hennedy discloses, according to claim 7 above, the limitations of the claim including a first shift register, a second shift register, a selector unit, and a control unit. Further, Hennedy discloses according to figure 1 that a received signal (SIGNAL INPUT) is divided into first (in-phase) and second (quadrature) signals (outputs of mixers 31 and 32) and each divided signal is sampled by a sampler (33 and 34). Hennedy further discloses, according to the illustrations of figure 1 and 8, that the first and second divided signals become the first and second received signals

(fig. 8; I SIGNAL REG and Q SIGNAL REG, respectively) after being sampled. Where the first and second (fig. 1, outputs of mixers 31 and 32) signals are components of the "SIGNAL INPUT" of figure 1, they are obviously considered to be "oversampled" by the two sampling analog to digital converters (fig. 1, refs. 33 and 34) because they are sampled *two-fold* with respect to the single SIGNAL INPUT and are picked every few samples of the composite SIGNAL INPUT to create the two sequences of the first and second received signals (outputs of the analog to digital converters 33 and 34, respectively). Additionally, the correlation calculations of the first received signal and the second received signal are performed by use of a common de-spreading code (fig. 8, output of DATA REFERENCE SIGNAL REGISTER).

Allowable Subject Matter

1. Claims 4-6 are indicated to contain allowable subject matter.

2. The following is a statement of reasons for the indication of allowable subject matter:

Claims 4-6 are indicated to contain allowable subject matter because the prior art of record does not anticipate or obviate all the features of independent claims 4 and 6. In particular, the prior art of record does not disclose the first and second sequence order control circuits to rearrange the received signal sequences and corresponding delay profiles of claim 4, and the prior art of record does not disclose the N received signal holding units and the selector to select one of the N received signal holding units to apply to a one of the plurality of received signal registers of claim 6.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
September 8, 2005

jmp

CHIEH M. FAN
PRIMARY EXAMINER